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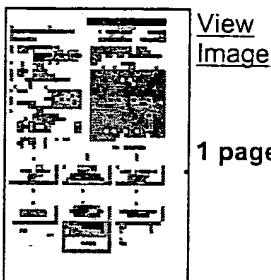
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Get Now:  PDF | More choices...Tools: Add to Work File:  Create new Work File  AddView: Jump to: [Top](#)Go to: [Derwent](#)[Email this to a friend](#)Title: **JP01117363A2: VERTICAL INSULATED GATE FIELD EFFECT TRANSISTOR**Derwent Title: Vertical-structure insulated-gate field-effect transistor - has conduction well region on high-concentration impurity region with conduction type same as drain NoAbstract Dwg 1/7 [\[Derwent Record\]](#)

Country: JP Japan

Kind: A



Inventor: TAKAO NORIYUKI;

Assignee: NEC CORP  
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Published / Filed: 1989-05-10 / 1987-10-30

Application Number: JP1987000275261

IPC Code: H01L 29/78;

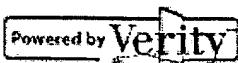
Abstract: PURPOSE: To realize a longitudinal IGFET wherein a parasitic transistor does not readily operate in the absence of an increase in ON-resistance by a method wherein a second semiconductor region of one conductivity type higher in impurity concentration than a first semiconductor region is formed on the lower section of a well region in contact with a drain region.

CONSTITUTION: In contact with a drain region 6 positioned under a well region 2, a high-concentration second semiconductor region 1 is formed, which is same as the drain region 6 in conductivity type. In such a design, breakdown strength is lower in the second semiconductor region 1 than in the surface, which causes a breakdown current to flow not on the surface but through the second semiconductor region 1. No parasitic transistor operates because there is no current in a base resistor, which contributes to the prevention of a thermal runaway. There is no increase in ON-resistance because there is no change in the gate width.

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Family: None

Other Abstract Info: None

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